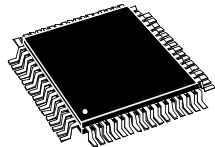


USB 2.0 high-speed Flash drive controller

Features

- USB 2.0 interface compatible with mass storage device class
 - Integrated USB 2.0 PHY
 - Supports USB high speed and full speed
 - Suspend and Resume operations
 - Mass storage controller interface (MSCI)
 - Supports all types of NAND Flash devices including ST, Hynix, Samsung, Toshiba, Renesas, and Micron
 - Reed-Solomon encoder/decoder: on-the-fly correction (4 bytes of a 512-byte block)
 - Flash identification support
 - Up to 21 Mbyte/s for read and 11 Mbyte/s for write operations in dual channel
 - Embedded ST7 8-bit MCU
 - Supply management
 - 3.3V operation
 - Integrated 3.3 -1.8 V voltage regulator
 - USB 2.0 low-power device compliant
 - Less than 100 mA during write operation with two NAND Flash devices
 - Less than 500 μ A in suspend mode
 - Clock management
 - Integrated PLL for generating core and USB 2.0 clock sources using external 12 MHz crystal
- 

LQFP64 10x10

 - AutoRun CDROM partition support
 - Data protection
 - Write protect switch control
 - Public/Private partitions support
 - Bootability support (HDD mode)
 - Production tool device configurability:
 - USB vendor ID/product ID (VID/PID), serial number and USB strings with foreign language support
 - SCSI strings
 - One or two LED outputs
 - Adjustable NAND Flash bus frequency to reach highest performance
 - Code update in the NAND Flash
 - LQFP64 10x10 lead-free package
 - Development support
 - Complete reference design including schematics, BOM and gerber files
 - Supports Windows (Vista, XP, 2000, ME), Linux and MacOS. Drivers available for Windows 98 SE

Table 1. Device summary

Features	Orderable part numbers	
	ST72682/R20	ST72682/R21
USB interface	USB 2.0 high speed	
Number of NAND devices supported	up to 8	
Read/write speed	21MBps/11MBps	
Operating supply	3.0 to 3.6 V	
Operating Temperature	0°C to +70°C	
Package	LQFP64 10x10 / die form	

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1 Introduction

The ST72682 is a USB 2.0 high-speed Flash drive controller. The USB 2.0 high-speed interface includes PHY and function and supports USB 2.0 mass storage device class.

The Mass storage controller interface (MSCI), combined with the Reed-Solomon encoder/decoder on-the-fly correction (4 bytes on 512-byte data blocks), provides a flexible high transfer rate solution for interfacing a wide of range NAND Flash memory devices.

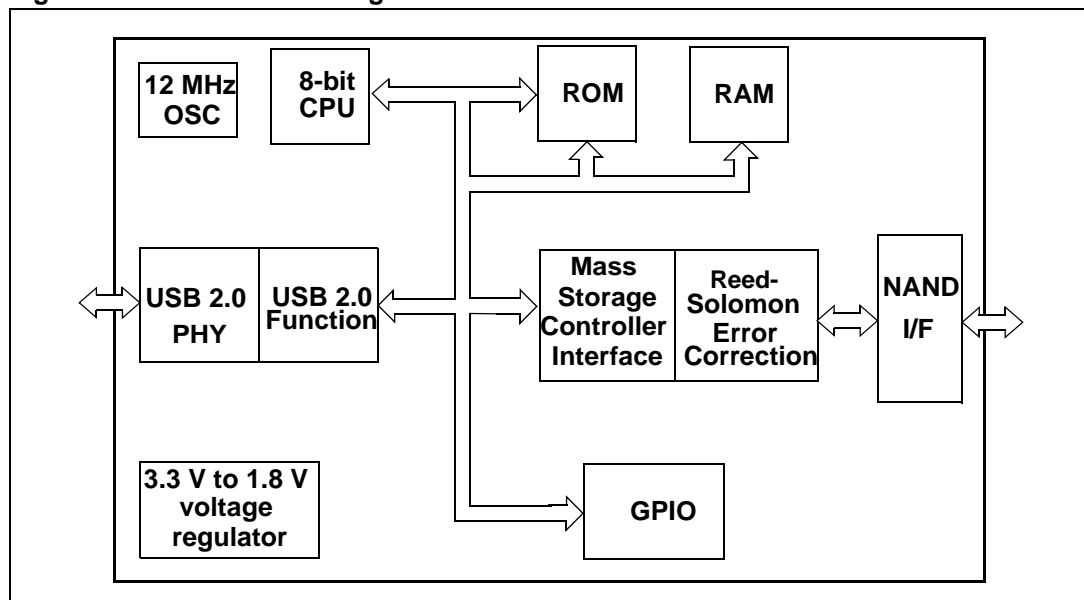
The internal 60 MHz PLL driven by the 12 MHz oscillator is used to generate the 480 MHz frequency required for the USB 2.0 PHY.

The ST7 8-bit CPU runs the application program from the internal ROM and RAM. USB data and patch code are stored in internal RAM.

The I/O ports provide allow to connect EEPROM, LEDs and a write protect switch control.

The internal 3.3 V to 1.8 V voltage regulator provides the 1.8 V supply voltage to the digital part of the circuit.

Figure 1. Device block diagram



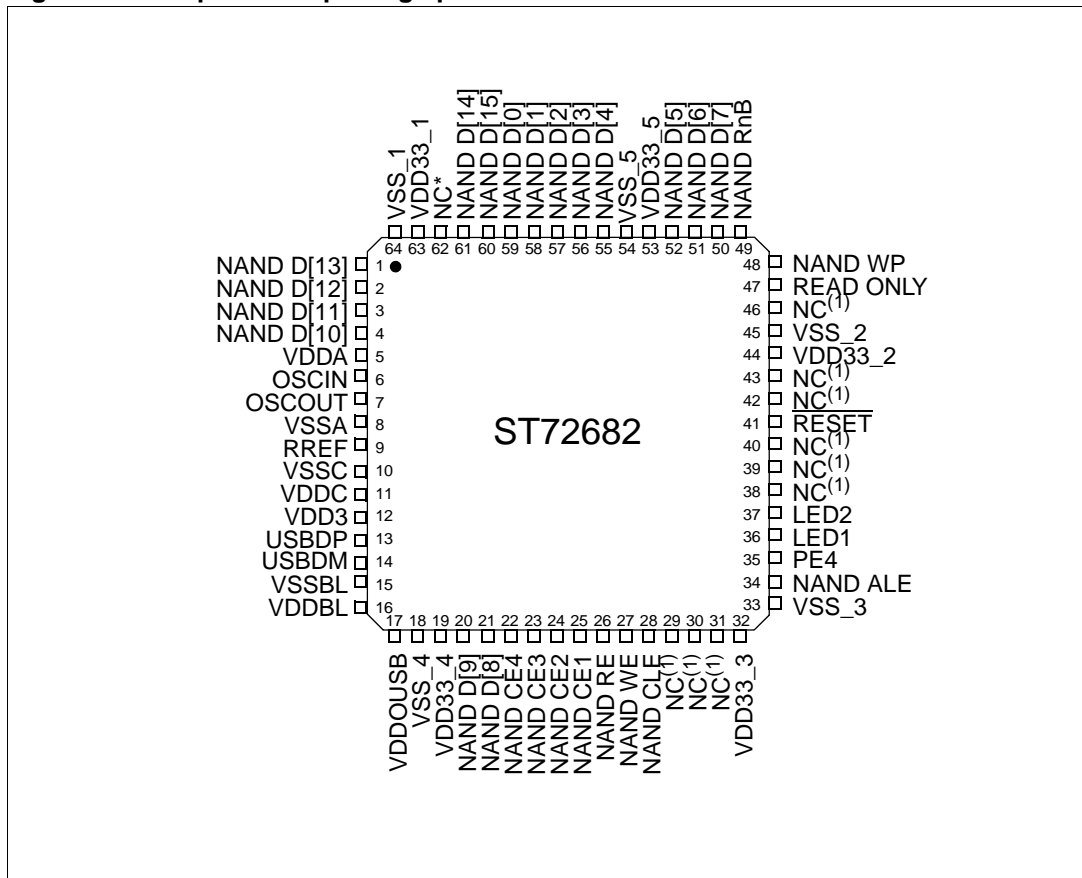
2 Pin description

Figure 2 shows the LQPF64 package pinout, while Table 2, Table 3, Table 4, Table 5, and Table 6 give the pin description.

The legend and abbreviations used in these tables are the following:

- Type
 - I = input
 - O = output
 - S = supply
- Input level: A = Dedicated analog input
- In/Output level
 - $C_T = \text{CMOS } 0.3V_{DD}/0.7V_{DD}$ with input trigger
 - $T_T = \text{TTL } 0.8V / 2V$ with Schmitt trigger
- Output level
 - D8 = 8mA drive
 - D4 = 4mA drive
 - D2 = 2mA drive

Figure 2. 64-pin LQFP package pinout



1. Must remain NOT connected in the application.

Table 2. Power supply pins

Pin	Pin name	Type	Description
LQFP64			
64	VSS_1	S	Ground
63	VDD33_1	S	I/Os and regulator supply voltage
45	VSS_2	S	Ground
44	VDD33_2	S	I/Os and regulator supply voltage
33	VSS_3	S	Ground
32	VDD33_3	S	I/Os and regulator supply voltage
18	VSS_4	S	Ground
19	VDD33_4	S	I/Os and regulator supply voltage
54	VSS_5	S	Ground
53	VDD33_5	S	I/Os and regulator supply voltage
17	VDDOUSB	O	USB2 PHY, OSC and PLL power supply output (1.8V)

Table 3. Control and system

Pin	Pin name	Type	Power	Level		Description
				Input	Output	
41	RESET	I/O	3.3	C _T		Reset input with filter with internal pull-up

Table 4. USB 2.0 Interface

Pin	Pin name	Type	Description
LQFP64			
16	VDDBL	S	Supply voltage for buffers and deserialisation flip flops (1.8 V)
15	VSSBL	S	Ground for buffers and deserialisation flip flops (1.8 V)
14	USBDM	I/O	USB2 DATA -
13	USBDP	I/O	USB2 DATA +
12	VDD3	S	Supply voltage for the FS compliance (3.3 V)
11	VDDC	S	Supply voltage for DLL & XOR tree (1.8 V)
10	VSSC	S	Ground for DLL & XOR tree (1.8 V)
9	RREF	I/O	Ref. resistor for integrated impedance process adaptation (11.3 kOhms 1% Pull Down)

Table 5. USB 2.0 and core clock system

Pin	Pin name	Type	Description
LQFP64			
8	VSSA	S	Ground for oscillator & PLL (1.8 V)
7	OSCOOUT	O	12MHz oscillator output
6	OSCIN	I	12MHz oscillator input
5	VDDA	S	Supply voltage for oscillator & PLL (1.8 V)

Table 6. General Purpose I/O ports / Mass Storage I/Os

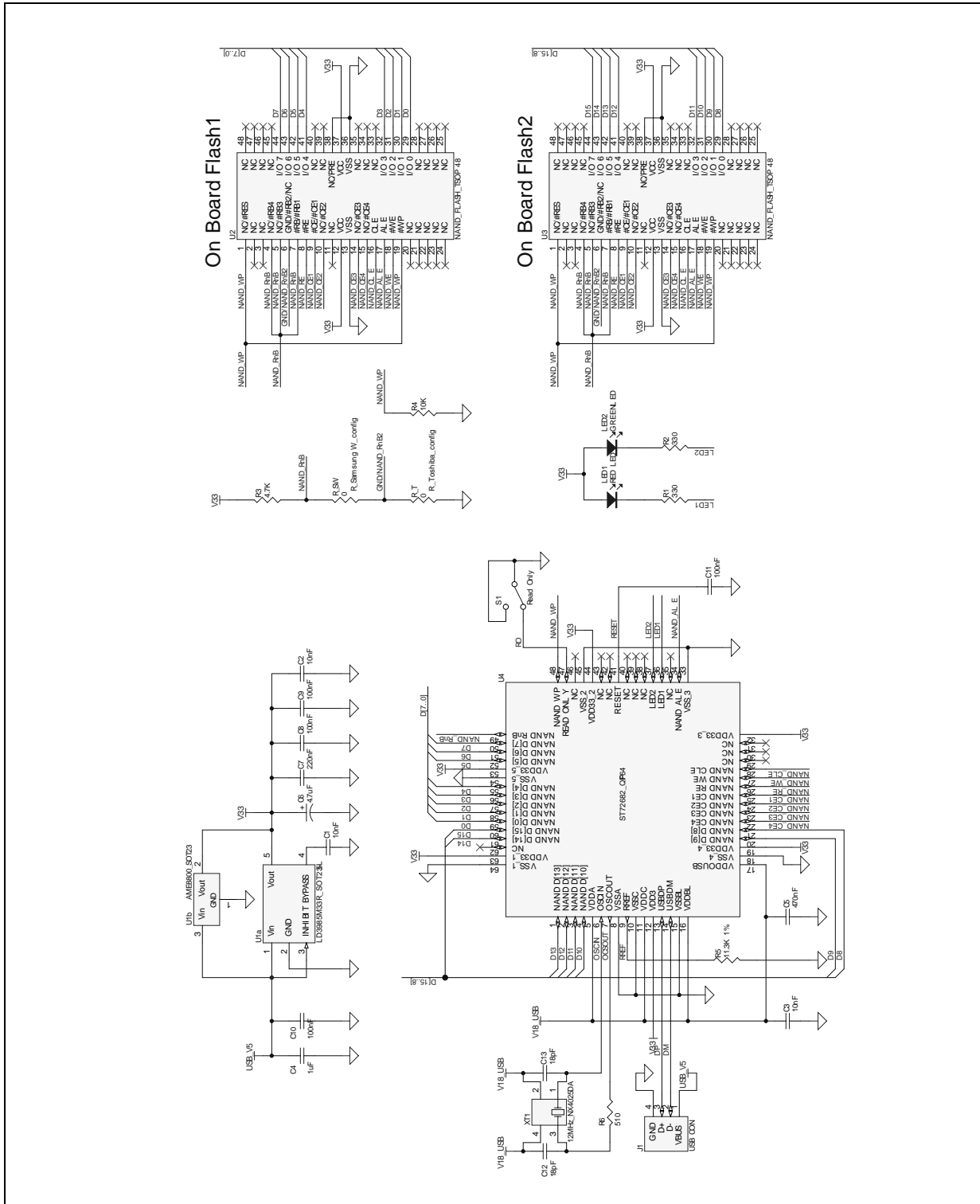
Pin	Pin name	Type	Level		Main function (after reset)
			Input	Outputs	
59	NAND D[0]	I/O	TT	D4	NAND data [0]
58	NAND D[1]	I/O	TT	D4	NAND data [1]
57	NAND D[2]	I/O	TT	D4	NAND data [2]
56	NAND D[3]	I/O	TT	D4	NAND data [3]
55	NAND D[4]	I/O	TT	D4	NAND data [4]
52	NAND D[5]	I/O	TT	D4	NAND data [5]
51	NAND D[6]	I/O	TT	D4	NAND data [6]
50	NAND D[7]	I/O	TT	D4	NAND data [7]
21	NAND D[8]	I/O	TT	D4	NAND data [8]
20	NAND D[9]	I/O	TT	D4	NAND data [9]
10	NAND D[10]	I/O	TT	D4	NAND data [10]
11	NAND D[11]	I/O	TT	D4	NAND data [11]
12	NAND D[12]	I/O	TT	D4	NAND data [12]
13	NAND D[13]	I/O	TT	D4	NAND data [13]
14	NAND D[14]	I/O	TT	D4	NAND data [14]
15	NAND D[14]	I/O	TT	D4	NAND data [15]
34	NAND ALE	I/O	TT	D8	NAND address latch enable
35	PE4	I/O	TT	D2	
28	NAND CLE	O	TT	D8	NAND command latch enable
27	NAND WE	O	TT	D8	NAND write enable
26	NAND RE	O	TT	D8	NAND read enable
25	NAND CE1	O	TT	D4	NAND enable 1
24	NAND CE2	O	TT	D4	NAND enable 2
23	NAND CE3	O	TT	D4	NAND enable 3

Table 6. General Purpose I/O ports / Mass Storage I/Os (continued)

Pin LQFP64	Pin name	Type	Level		Main function (after reset)
			Input	Outputs	
22	NAND CE4	O	TT	D4	NAND enable 4
49	NAND RnB	I	TT	D2	NAND Ready/ $\overline{\text{Busy}}$
48	NAND WP	O	TT	D2	NAND Write Protect
47	READ ONLY	I	TT	D2	Read-only switch (“0”: Read/Write; “1”: Read only)
	EEPROM SCL	O	TT	D2	EEPROM serial clock
37	LED2	O	TT	D8	Green LED (USB access)
36	LED1	O	TT	D8	Red LED (NAND access)

3 Application schematics

Figure 3. Application schematic



4 NAND Flash memory interface

[Table 7](#) gives the list of NAND Flash memory devices compatible with ST72682/R20 and ST72682/R21 devices. This list is only provided as a guide as it is not possible to automatically guarantee support for all the additions and updates across the listed ranges of manufacturers' devices.

Table 7. Known NAND Flash memory compatibility guide for ST72682/R20 and ST72682/R21

NAND Flash part number	NAND Flash size (Mbytes or Gbytes) and type	Number of NAND Flash devices supported	
		ST72682/R20 device	ST72682/R21 device
Samsung K9F1G08U	128 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9F2G08U	256 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9F4G08U	512 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9K4G08U	512 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9W4G08U	512 MB; SLC2K; Dual CE	2 or 4	1, 2 or 4
Samsung K9K8G08U	1 GB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9W8G08U	1 GB; SLC2K; Dual CE	2 or 4	1, 2 or 4
Samsung K9WAG08U	2 GB; SLC2K; Dual CE	2 or 4	1, 2 or 4
Samsung K9NBG08U	4 GB; SLC2K; Quad CE	2	1 or 2
Samsung K9G4G08U	512 MB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9L8G08U	1 GB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Samsung K9HAG08U	2 GB; MLC2K; Dual CE	2 or 4	1, 2 or 4
Samsung K9MBG08U	4 GB; MLC2K; Quad CE	2	1 or 2
Toshiba TH58NVG0S3	128 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Toshiba TH58NVG1S3	256 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Toshiba TH58NVG2S3	512 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Toshiba TH58NVG1D4	256 MB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Toshiba TH58NVG2D4	512 MB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Toshiba TH58NVG3D4	1 GB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
ST NAND01GW3B	128 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
ST NAND02GW3B	256 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
ST NAND04GW3B	512 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
ST NAND08GW3B	1 GB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
ST NAND04GW3C	512 MB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Hynix HY27UF081G2M	128 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Hynix HY27UG082G2M	256 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Hynix HY27UG084G2M	512 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Hynix HY27UH084G5M	512 MB; SLC2K; Dual CE	2 or 4	1, 2 or 4

Table 7. Known NAND Flash memory compatibility guide for ST72682/R20 and ST72682/R21

NAND Flash part number	NAND Flash size (Mbytes or Gbytes) and type	Number of NAND Flash devices supported	
		ST72682/R20 device	ST72682/R21 device
Hynix HY27UH088G2M	1 GB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Hynix HY27UT084G2M	512 MB; MLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Hynix HY27UU088G5M	1 GB; MLC2K; Dual CE	2 or 4	1, 2 or 4
Micron 29F2G08AA	256 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Micron 29F4G08BA	512 MB; SLC2K; Single CE	1, 2, 4, 6 or 8	1, 2, 4, 6 or 8
Micron 29F8G08FA	1 GB; SLC2K; Dual CE	2 or 4	1, 2 or 4

4.1 NAND Flash error correction

No NAND Flash memory arrays are guaranteed by manufacturers to be error-free. Error occurrence depends on the Flash cell type (MLC or SLC).

The ST72682 embeds hardware and firmware mechanisms to correct the errors.

4.1.1 Hardware error correction

The ST72682 embeds a Reed-Solomon algorithm-based hardware cell. This cell directly manages 512-byte data packets on the NAND I/O system.

Based on the data packet content, the cell generates an 80-bit Error Correction Code (ECC) consisting of 8 words, each containing 10 bits.

During write operations to NAND memory, the 512-bytes of data and the ECC are stored together in the same page. The ECC is stored in the corresponding Redundant Area (RA), using 10 bytes.

During read operations, the 512-bytes of data and the 8 ECC words are read back and are passed through the Reed-Solomon cell for decoding. The cell allows the correction of 4 symbols in this 520-symbol packet (512 symbols from data + 8 symbols from ECC).

The hardware cell gives three possible results:

- No error detected: the data packet can be used as it is.
- Correctable error detected: the corrected data are available in a specific 512-byte buffer in the Reed-Solomon cell and are ready to be used.
- Uncorrectable error detected: data corruption cannot be repaired.

4.1.2 Firmware error management

The firmware defines the error correction possibilities with the corrected data packet.

When data cannot be repaired, the block is considered as a bad block and is replaced by another one. See [Section 4.2](#) for further information on bad block management.

4.2 Bad block management

NAND memory manufacturers deliver their devices with factory-marked bad blocks. This marking depends on the manufacturer and the NAND memory type (page size, memory technology, etc.). The ST72682 supports all bad block markings currently available on the market.

4.2.1 Bad Block identification

During firmware initialization, the MCU scans the entire NAND memory configuration to identify bad blocks.

A bad block is defined as follows:

- Five different block status bytes are considered: 4 status bytes from page 0 and 1 from an other page (page 127 for MLC NAND; page 1 for SLC NAND).
- The considered block is marked as a bad block if one out of these five bytes contains at least four bits set to '0'.

4.2.2 Bad block replacement

The firmware works on groups of 1024 blocks, called zones. A complete NAND configuration can contain several zones:

- Each zone is described in a Look Up Table (LUT) containing 1024 entries. A LUT is composed of 3 parts: used blocks, free blocks and bad blocks.
- The "bad blocks" part contains as many entries as the number of bad blocks identified in that zone.
- The "used blocks" part can have a size of 1000, 900 or 500 entries. This size is configurable and also depends on the number of identified bad blocks.
- The "free blocks" part contains the remaining entries.

The used blocks part is used to do a correspondence between NAND blocks and logical address ranges.

This system allows all bad blocks to be masked from the Host. As a result, bad blocks are never seen. Only a range of logical addresses are visible which correspond to the sum of the used blocks part of all zones.

4.2.3 Late Fail block

During normal application life, defects may appear in the NAND memory. Under certain conditions, these defects are not correctable and the corresponding block is declared as "bad".

In this case, new bad blocks are identified in the bad blocks part of the LUT and replaced by new blocks from the "free blocks" part.

4.3 Wear levelling

During normal application life, the NAND memory is written and erased (at block level) many times. The NAND device is guaranteed for a limited number of write operations (about 100 000 cycles). As a consequence, the controller must keep write/erase operations to a minimum for any individual block.

A method to limit these cycles is to use a “Wear Levelling” scheme between all NAND memory blocks.

LUT usage

The LUT is used for transfers between a logical address range and a block. It contains free blocks which are used in the “wear levelling” scheme.

During write command treatment, the firmware calculates the zones, blocks and pages for data write access. In a block write operation, the firmware applies the following scheme to avoid block wearing:

- The least recently-used block is chosen from the free block part of the LUT.
- Valid data from the old block is copied to the new block.
- New data from the write command is written to the new block.
- The old block is erased.
- The LUT is updated after identifying the new block in the used block part and the old block in the free block part.

Using this scheme, a logical address range doesn't correspond to a constant block. A write command repeated several times to the same logical address writes physically into different blocks.

This method shares the wearing evenly across all blocks of the concerned zone.

4.4 NAND Flash interface configuration

Applications based on ST72682 can be configured through a dedicated PC software tool.

The NAND memory RE and WE signals frequencies can be independently configured to 30 MHz, 20 MHz, 15 MHz, 12 MHz and 10 MHz.

The logical size reduction factor can be configured to 90% or 50% in the event of having too many bad blocks. this option resizes the used blocks part of the LUT to 900 or 500.

5 Mass storage implementation

5.1 USB characteristics

The ST72682 is compliant with USB 2.0 specification.

It is able to operate in both high speed and full speed modes using a bidirectional control endpoint 0 and a bidirectional bulk endpoint 2.

It automatically recognizes the speed to use on the bus by a process of negotiation with USB Host.

5.2 BOT/SCSI implementation

5.2.1 BOT specification

The USB Mass Storage Class Bulk Only Transport (BOT) specification version 1.0 is implemented. It allows the device to be recognized by the host as a mass-storage USB device.

5.2.2 SCSI specification

Moreover, inside BOT transfers, SCSI commands are encapsulated for mass storage operations.

The related specifications are SBC-2 revision 10 (SCSI Block Commands 2) and SPC-4 revision 7a (SCSI Primary Commands 4).

5.2.3 Bootability specification

The USB mass storage specification for bootability revision 1.0 is implemented.

It allows the PC host to boot the operating system from the USB mass storage application. In this case, the Host uses BOT LUN 0 (logical unit number).

A specific tool must be used to format the logical drive in order to make it bootable by programming the correct information.

5.3 Multi-LUN device characteristics

The application can be configured with a dedicated PC software tool as a multi-LUN device.

In this case, up to 3 different drives are available: public drive, additional drive and private drive.

Public and additional drives can be configured as removable drive, hard disk drive or CD-ROM drive.

5.3.1 Public drive

The public drive is the default configuration in a mono-LUN mode. In this default case, it is declared as a removable drive.

The public drive is mandatory and can not be removed from the configuration. By customization (using PC software), it can be declared as a removable drive, a CD-ROM drive or a hard disk drive.

This drive is the LUN 0 in BOT commands.

5.3.2 Private drive

The Private drive is optional. Its type is “removable drive” and is not configurable.

This drive is protected by password and cannot be directly accessed through the PC operating system. A PC software tool is necessary to send a command with the password to unlock the device. The device is then open and accessible by the PC operating system until reset or reception of a new command to lock the drive.

This drive is the LUN 1 in BOT commands.

5.3.3 Additional drive

The additional drive is optional. Its type can be “removable drive”, “hard disk drive” or “CD-ROM drive”.

This drive is LUN 1 in BOT commands if the private drive option is not active, and is LUN 2 if the private drive option is active.

5.3.4 CD-ROM considerations

When a drive is declared as CD-ROM, the ST72682/R21 manages this drive with a logical block size of 2 Kbytes. To be correctly recognized by the host, it is preferable to build a CDFS partition on this CD-ROM. See the ‘ST7268x Production Tool User Manual’ for more information.

Note that the ST72682/R20 doesn’t consider the CD-ROM partition as a specific case. The logical block size is 512 bytes and any file system can be used.

In both cases, the CD-ROM partition allows the use of the AutoRun operating system feature. During device connection, the CD-ROM partition is recognized and the host tries to run the application corresponding to the autorun.inf file present into this CD-ROM partition.

5.4 Mass storage interface configuration

In addition to the parameters already described as configurable in the previous chapters, additional customizable information includes:

- USB parameters: VID, PID, all string information.
- SCSI parameters: strings for inquiry commands.

6 Human interface implementation

6.1 LED behavior

The application is designed to manage 2 LEDs. This behavior is configurable through PC dedicated software: 'ST7268x Production Tool'.

By default, LED 1 responds to NAND memory access activity and LED 2 responds to USB activity.

Use of LED 1 is optional. When this option is not active, LED 2 reacts to both USB and NAND memory activity.

6.2 Read-only switch

The READ ONLY pin of the ST72682 is an input pin to be connected to VDD or GND depending on the behavior of the device.

- When this pin is connected to GND, no limitations are applied on the PC command received.
- When this pin is connected to VDD or unconnected, the firmware filters all accesses to the NAND memory which modify the NAND memory state (write, erase, etc.) and returns an error to the PC.

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the Devices with an ambient temperature at $T_A=25\text{ °C}$ and $T_A=T_A\text{ max}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean}\pm 3\Sigma$).

7.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A=25\text{ °C}$, $V_{DD33}=3.3\text{ V}$. They are given only as design guidelines and are not tested.

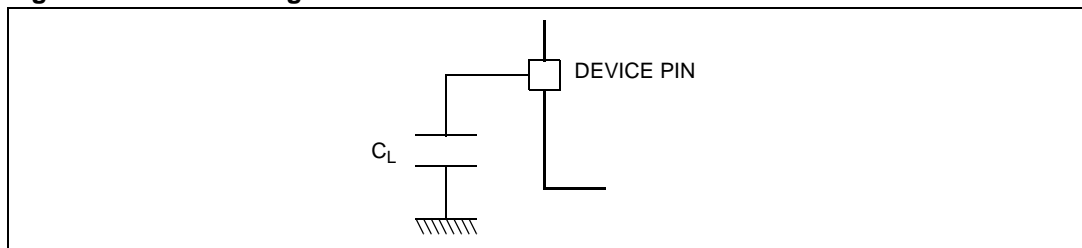
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 4](#).

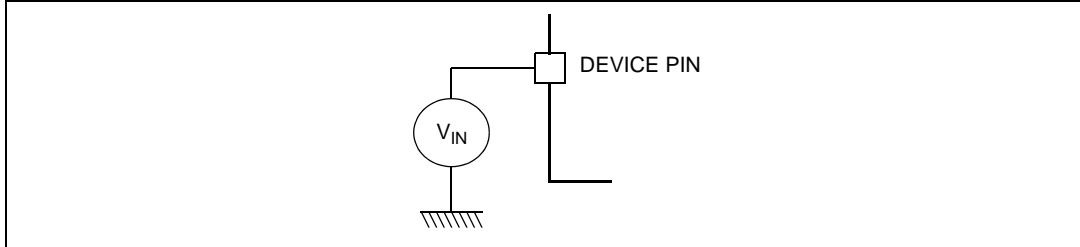
Figure 4. Pin loading conditions



7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 5](#).

Figure 5. Pin input voltage



7.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the Device. This is a stress rating only and functional operation of the Device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
$V_{DD33} - V_{SS}$	Supply voltage	4.0	V
$V_{IN}^{(1)(2)}$	Input voltage on any other pin	$V_{SS}-0.3$ to $V_{DD33}+0.3$	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see Section 7.6.3: Absolute Maximum Ratings (Electrical Sensitivity)	

1. Directly connecting the RESET and I/O pins to V_{DD33} or V_{SS} could damage the Device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for RESET, 10kΩ for I/Os). For the same reason, unused I/O pins must not be directly tied to V_{DD33} or V_{SS} .
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN} > V_{DD33}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 9. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD33}	Total current into V_{DD33} power lines (source) ⁽¹⁾	200	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	200	
$I_{IO}^{(2)}$	Output current sunk by any I/O D2 type	25	
	Output current sunk by any I/O D4 type	35	
	Output current sunk by any I/O D8 type	50	
	Output current source by any I/Os and control pin	-25	

1. All power supply (V_{DD33}) and ground (V_{SS}) lines must always be connected to the external supply.
2. Refer to [Table 6](#) for the output drive capability of each of the I/Os.

Table 10. Thermal characteristics

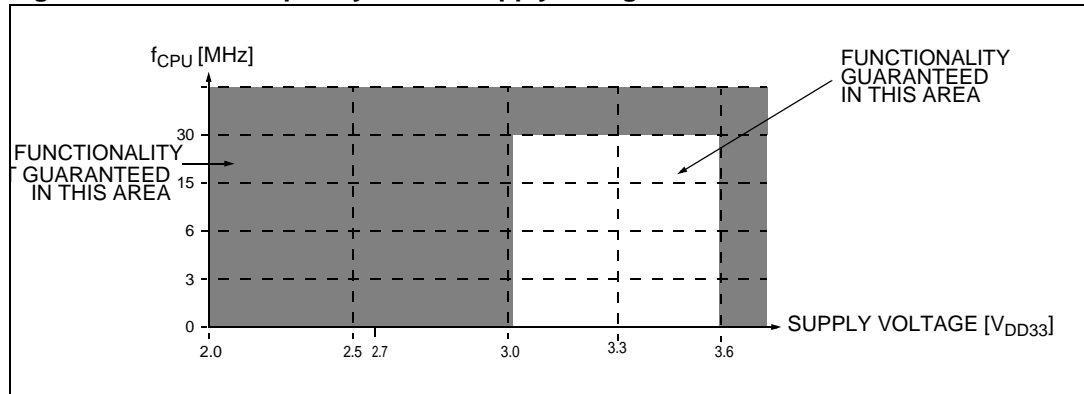
Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
T _{JMAX}	Maximum junction temperature	120	°C

7.3 Operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD33}	Power Supply		3.0	3.6	V
T _A	Ambient temperature range		0	70	°C

Figure 6. Clock frequency versus supply voltage



7.4 Supply current characteristics

Table 12. RUN and SUSPEND modes current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD}	Supply current in RUN mode	f _{OSC} =12MHz	15	25	35	mA
	Supply current in SUSPEND mode	V _{DD33} =3.3V, T _A =+25°C	60	90	190	µA

Table 13. Supply and Clock managers current

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽²⁾	Unit
I _{DD(CK)}	Supply current of crystal oscillator ⁽³⁾		1000	2000	µA

1. Typical data are based on T_A=25 °C and f_{CPU}=12 MHz.
2. Data based on characterization results, not tested in production.
3. Data based on characterization results done with the external components specified in [Section 7.5.1](#), not tested in production.

7.5 Clock and timing characteristics

Subject to general operating conditions for V_{DD33} , f_{OSC} , and T_A .

7.5.1 Crystal oscillator

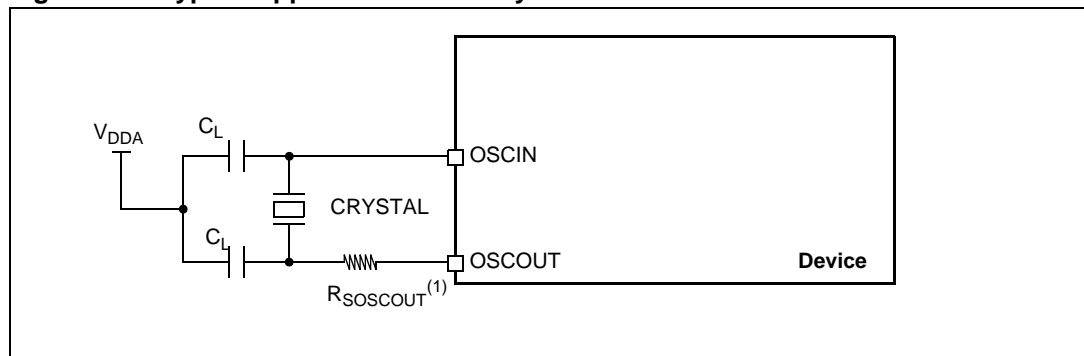
The Device internal clock is supplied from a crystal oscillator. All the information given in this paragraph are based on characterization results with specified typical external components. In the application the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal manufacturer for more details (frequency, package, accuracy...).

Table 14. Clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency			12		MHz
CK_{ACC}	Total crystal oscillator accuracy	Absolute value + temperature + aging			± 60	ppm
α_{OSC}	Crystal oscillator duty cycle ⁽¹⁾		45	50	55	%

1. The crystal oscillator duty cycle has to be adjusted through the two C_L capacitors. Refer to the crystal manufacturer for more details.

Figure 7. Typical application with a crystal



1. Depending on the crystal power dissipation, a serial resistor $R_{SOSCOUT}$ may be added. Refer to the crystal manufacturer for more details.

Table 15. Typical C_L and R_S values by crystal

Supplier	Typical Crystal	C_L (pF)	$R_{SOSCOUT}$ (Ω)
NDK	AT51 or AT41	16	560

7.6 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

7.6.1 Functional EMS (Electromagnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD33} and V_{SS33} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations
 - The software flowchart must include the management of runaway conditions such as:
 - Corrupted program counter
 - Unexpected reset
 - Critical Data corruption (control registers...)
- Prequalification trials
 - Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.
 - To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 16. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD33}=3.3\text{ V}$, $T_A=+25\text{ °C}$, $f_{OSC}=12\text{ MHz}$ compliant with IEC 1000-4-2	4B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD33} and V_{SS33} pins to induce a functional disturbance	$V_{DD33}=3.3\text{ V}$, $T_A=+25\text{ °C}$, $f_{OSC}=12\text{ MHz}$ compliant with IEC 1000-4-4	4A

7.6.2 Electromagnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 17. EMI characteristics

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. (f _{osc} at 12 MHz)	Unit
S _{EMI}	Peak level	V _{DD33} =3.3 V, T _A =+25 °C, conforming to SAE J 1752/3 ⁽¹⁾	0.1 to 30 MHz	20	dBμV
			30 to 130 MHz	25	
			130 MHz to 1 GHz	25	
			SAE EMI Level	4	-

1. Refer to Application Note AN1709 for data on other package types.

7.6.3 Absolute Maximum Ratings (Electrical Sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic Discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Table 18. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (Human Body Model)	T _A =+25°C	2000	V

1. Data based on characterization results, not tested in production.

Static and Dynamic Latch-Up

- **LU:** 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU:** Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 19. Electrical sensitivities

Symbol	Parameter	Conditions	Class ⁽¹⁾
LU	Static latch-up class	T _A =+25 °C	A
DLU	Dynamic latch-up class	V _{DD33} =3.3 V, f _{OSC} =12 MHz, T _A =+25 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

7.7 I/O port pin characteristics

7.7.1 General characteristics

Subject to general operating conditions for V_{DD33}, f_{OSC}, and T_A unless otherwise specified.

Table 20. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	Input low level voltage ⁽¹⁾	TTL ports	0.85V _{DD33}		0.16V _{DD33}	V
V _{IH}	Input high level voltage ⁽¹⁾					
V _{hys}	Schmitt trigger voltage hysteresis ⁽²⁾				400	mV
I _L	Input leakage current	V _{SS} ≤ V _{IN} ≤ V _{DD33} , standard I/Os			1	µA
R _{PU}	Weak pull-up equivalent resistor ⁽¹⁾	V _{IN} =V _{SS} V _{DD33} = 3.3 V	32	50	75	kΩ

1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, tested in production at V_{DD33} max.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

Figure 8. Two typical applications with unused I/O pin

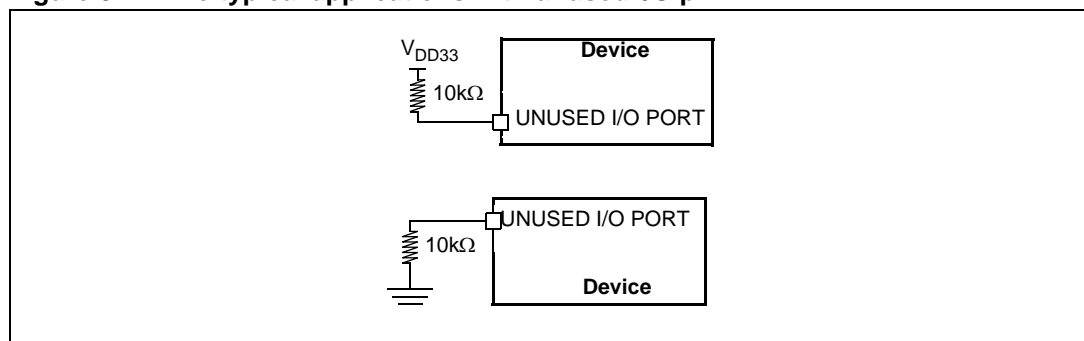


Figure 9. Typical V_{IL} and V_{IH} standard I/Os

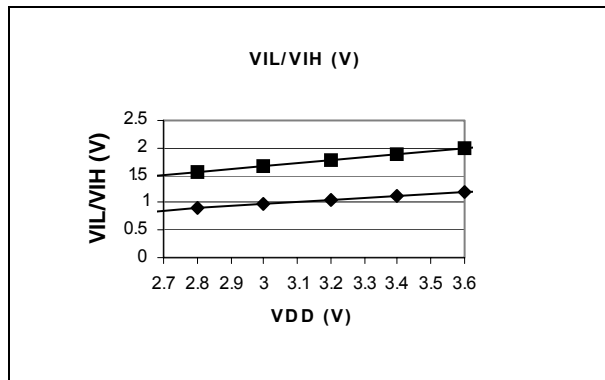
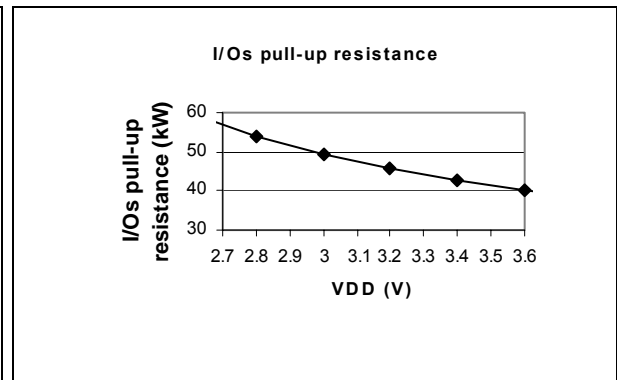


Figure 10. Typical R_{PU} vs. V_{DD33} with $V_{IN}=V_{SS}$



7.7.2 Output driving current

Subject to general operating conditions for V_{DD33} , f_{OSC} , and T_A unless otherwise specified.

Table 21. Output driving current

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for a D2 I/O pin when 8 pins are sunk at same time (see Figure 11)	$I_{IO}=2mA$		300	mV
	Output low level voltage for a D4 I/O pin when 8 pins are sunk at same time (see Figure 12)	$I_{IO}=4mA$		400	
	Output low level voltage for a D8 I/O pin when 8 pins are sunk at same time (see Figure 13)	$I_{IO}=8mA$		500	
$V_{DD33}^{(2)}$ V_{OH}	Output high level voltage for a D2 I/O pin when 8 pins are sourced at same time (see and Figure 14)	$I_{IO}=2mA$		600	mV
	Output high level voltage for a D4 I/O pin when 8 pins are sourced at same time (see Figure 15)	$I_{IO}=4mA$		600	
	Output high level voltage for a D8 I/O pin when 8 pins are sourced at same time (see Figure 16)	$I_{IO}=8mA$		600	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Section Table 9](#). and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in [Section Table 9](#). and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD33} . True open drain I/O pins does not have V_{OH} .

Figure 11. Typical V_{OL} at $V_{DD33}=3.3 V$ (I/O D2) Figure 12. Typical V_{OL} at $V_{DD33}=3.3 V$ (I/O D4)

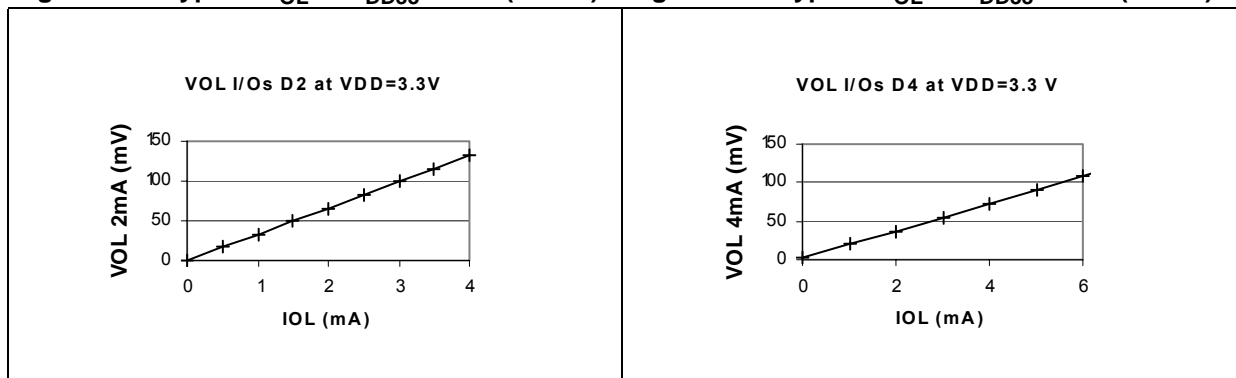


Figure 13. Typical V_{OL} at $V_{DD33}=3.3\text{ V}$ (I/O D8) Figure 14. Typical $V_{DD33}-V_{OH}$ vs. V_{DD33} (I/O D2)

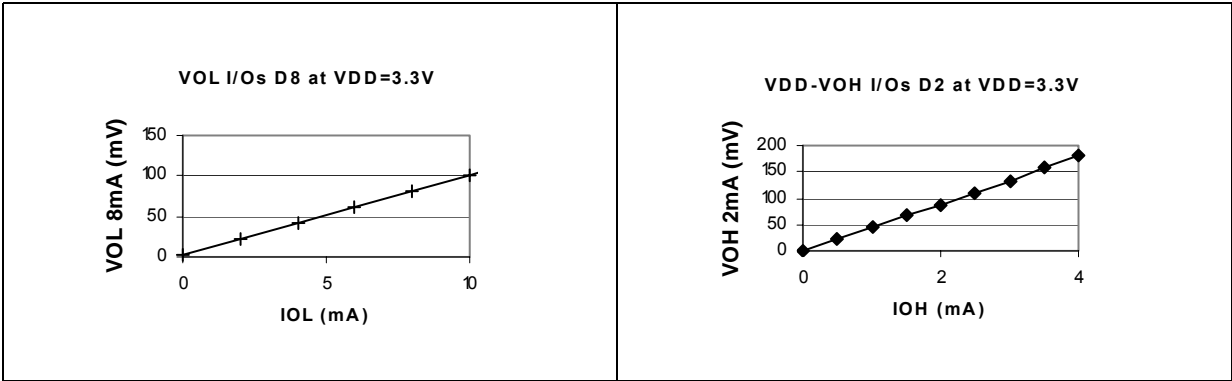
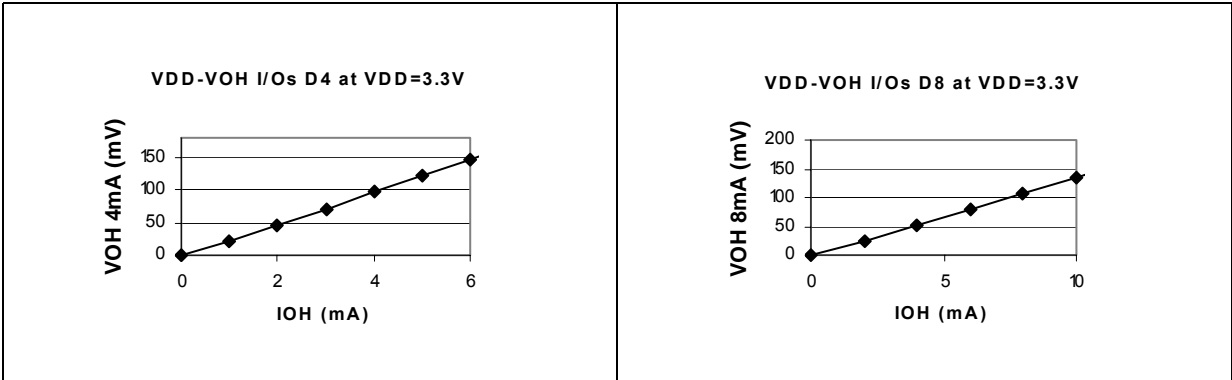


Figure 15. Typical $V_{DD33}-V_{OH}$ vs. V_{DD33} (I/O D4) Figure 16. Typical $V_{DD33}-V_{OH}$ vs. V_{DD33} (I/O D8)



7.8 Control pin characteristics

7.8.1 Asynchronous $\overline{\text{RESET}}$ pin

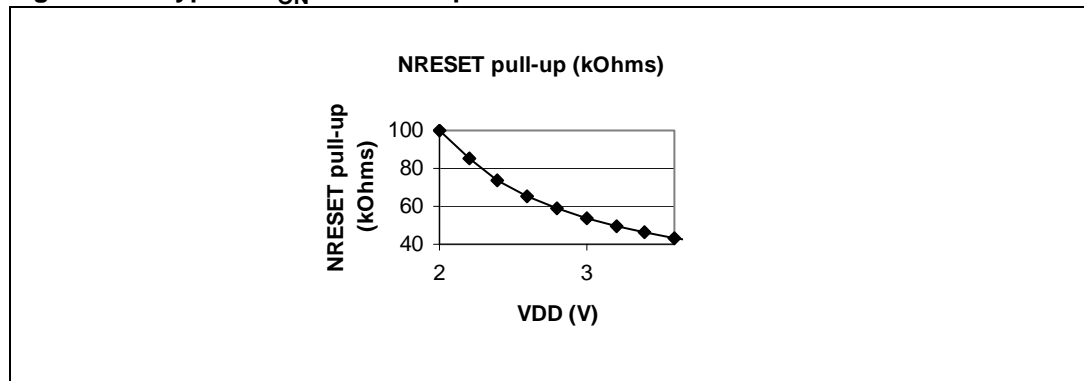
T_A ranges between 0 and +55 °C unless otherwise specified.

Table 22. Asynchronous $\overline{\text{RESET}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage ⁽¹⁾				$0.16V_{DD33}$	V
V_{IH}	Input high level voltage		$0.85V_{DD33}$			
V_{hys}	Schmitt trigger voltage hysteresis ⁽¹⁾			450		mV
R_{ON}	Pull-up equivalent resistor	$V_{DD33} = 3.3 \text{ V}$	20	40	80	k Ω
		$V_{DD33} = 2 \text{ V}$		100		
$t_{eh(RSTL)}$	External reset pulse hold time ⁽²⁾		2.5			μs
$t_{g(RSTL)}$	Filtered glitch duration ⁽³⁾			200		ns
$t_{ew(RSTL)}$	External reset pulse duration ⁽⁴⁾		500			μs
$t_{iw(RSTL)}$	Internal reset pulse duration			2		Tcpu

1. The level on the $\overline{\text{RESET}}$ pin must be free to go below the V_{IL} max. level specified in [Section 7.8.1](#). Otherwise the reset will not be taken into account internally.
2. To guarantee the reset of the Device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{eh(RSTL)}$ can be ignored. Not tested in production, guaranteed by design.
3. The reset network protects the device against parasitic resets.
4. The external reset duration must respect this timing to guarantee a correct start-up of the internal regulator at power-up. Not tested in production, guaranteed by design.

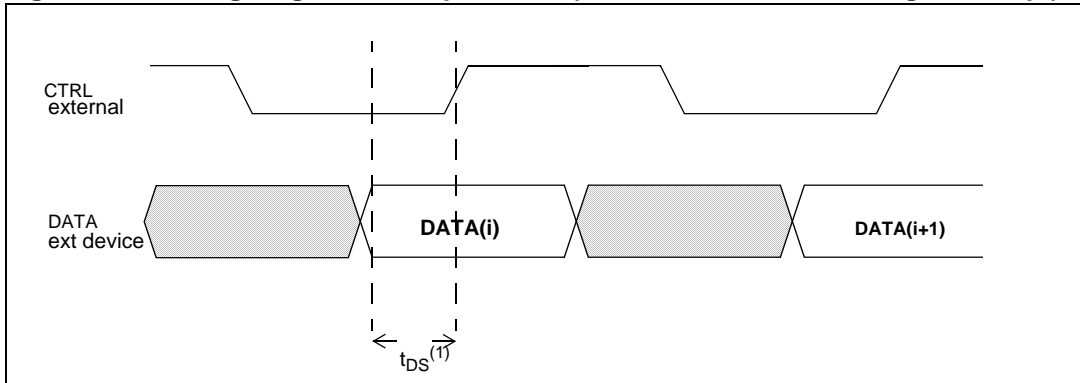
Figure 17. Typical R_{ON} on $\overline{\text{RESET}}$ pin



7.9 Other communication interface characteristics

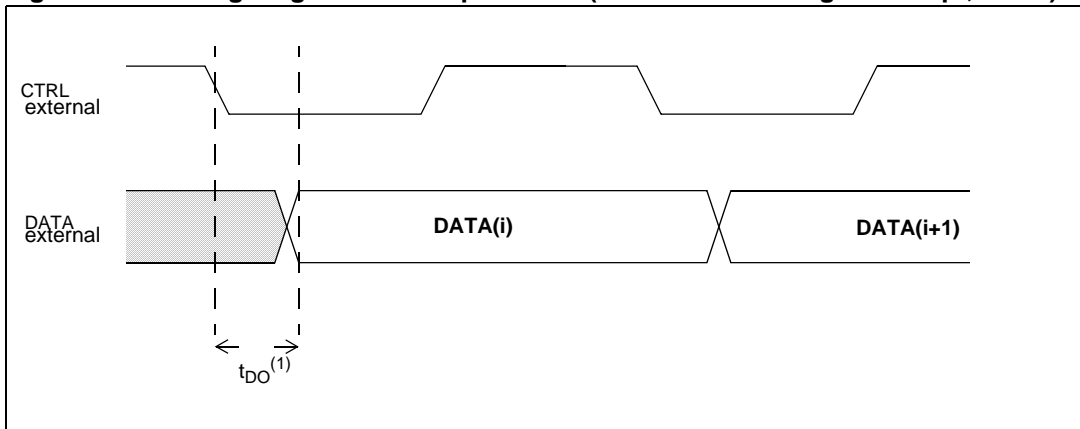
7.9.1 MSCI parallel interface

Figure 18. Timing diagrams for input mode (with max load on CTRL signal = 50 pf)



1. t_{DS} is the setup time for data sampling.

Figure 19. Timing diagrams for output mode (with max CTRL signal = 50 pf, DATA)



1. t_{DO} is the data output time for data sampling.

Table 23. MSCI parallel interface DC characteristics

MSCI DC Electrical Characteristics						
Parameter	Symbol	Conditions	Min.	Typ ⁽¹⁾	Max.	Unit
Data setup time	t_{DS}			11		ns
Data output time	t_{DO}			6		ns
CTRL line capacitance	Cctrl			50		pF
Data line capacitance	Cdata			50		pF

1. Data based on design simulation and not tested in production.

7.9.2 USB (Universal Bus Interface)

Table 24. USB Interface DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{DDsuspend}	Suspend current	V _{DD33} =3.3 V, regulator and PHY ON	0.5 ⁽¹⁾	1.5	6 ⁽¹⁾	mA
		V _{DD33} =3.3 V, Power-down mode, 25 °C ⁽²⁾	60	90	190	µA
R _{PU}	Pull-up resistor ⁽¹⁾			1.5		kΩ
Full Speed Mode						
V _{TERM}	Termination voltage		0.8		2.0	V
VOH	High level output voltage		2.8		3.6	V
VOL	Low level output voltage				0.8	V
V _{CRS}	Crossover voltage		1.3		2.0	V
High Speed Mode						
V _{HSH}	HS data signalling high			400		mV
V _{HSL}	HS data signalling low			5		mV

1. Not tested in production, guaranteed by characterization.
2. In order to reach this value, the software must force the regulator into power-down mode and the I/Os compensation cell off.

Table 25. USB Interface AC timing

Symbol	Parameter	Conditions	Min.	Max.	Unit
Full Speed Mode					
T _{FR}	Rise Time	C _L =50pF	4	20	ns
T _{FF}	Fall Time	C _L =50pF	4	20	ns
High Speed Mode					
T _{HSR}	Rise Time			500 ⁽¹⁾	ps
T _{HSF}	Fall Time			500 ⁽¹⁾	ps
T _{HSDRAT}	HS Data Rate		479.76	480.24	Mb/s

1. Not tested in production, guaranteed by characterization.

Figure 20. USB signal eye diagram

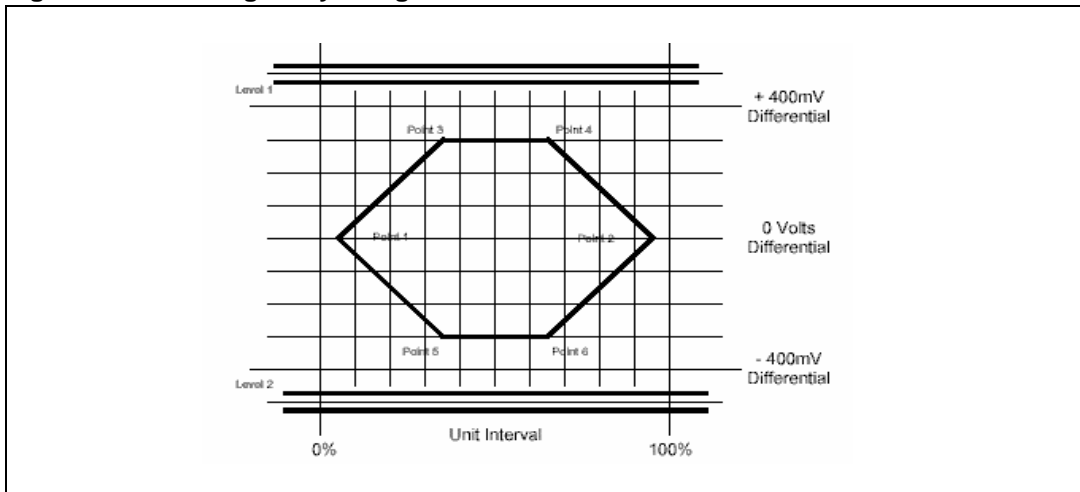


Table 26. USB high speed transmit waveform requirements

	Voltage Level (DP - DN)	Time
Unit Interval (UI)	-	2.082 to 2.084 ns
Level 1	475 mV	-
Level 2	-475 mV	-
Point 1	0 V	5% UI
Point 2	0 V	95% UI
Point 3	300 mV	35% UI
Point 4	300 mV	65% UI
Point 5	-300 mV	35% UI
Point 6	-300 mV	65% UI

8 Package mechanical data

Figure 21. 64-pin Thin Quad Flat Package (10 x10) package outline

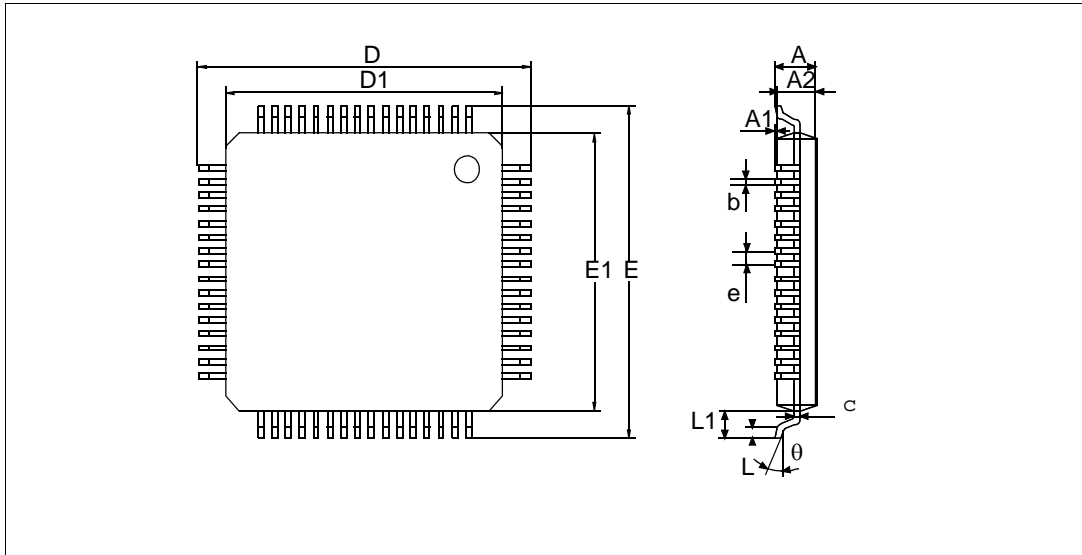


Table 27. 64-pin Thin Quad Flat Package (10 x10) mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of pins					
N	64					

9 Device ordering information

Table 28. Feature comparison

Features added in the ST72682/R21 versus ST72682/R20	Description
Continued AutoRun CDROM partition support	AutoRun runs a program when the USB Flash drive is inserted into a computer.

Table 29. Ordering Information

Orderable part number	Package	Operating voltage	Temperature range
ST72682/R20	LQFP64 10x10mm	3.0V to 3.6V	0°C to +70 °C
ST72682/R21 (latest firmware revision)	LQFP64 10x10mm	3.0V to 3.6V	0°C to +70 °C

10 Revision history

Table 30. Document revision history

Date	Revision	Description of Changes
09-Feb-2006	1.0	Initial release
14-Aug-2007	2.0	Firmware revision updated to R21. References to TQFP64 updated to LQFP64. Datasheet reformatted.

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